

A 900-MHz 1.5-V CMOS Voltage-Controlled Oscillator Using Switched Resonators With a Wide Tuning Range

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Abstract—A 900-MHz fully integrated VCO was fabricated in a 0.18- μ m foundry CMOS process. Under 1.5 V power supply, this VCO can be tuned from 667 MHz to 1156 MHz which corresponds to a 53.6% tuning range. The VCO has nearly constant phase noise over the whole tuning frequency, credit to the switched resonators used in this VCO. The phase noise at a 600 kHz offset is -123.1 dBc/Hz at 1125 MHz center frequency and -124.2 dBc/Hz at 667 MHz center frequency.

Index Terms—CMOS voltage-controlled oscillator, phase noise, switched resonators, tuning range.

I. INTRODUCTION

A MAJOR challenge for implementing a fully integrated transceiver is integrating a VCO. The stringent phase noise requirements in a standard like 802.11a make integration of a VCO risky. A potential approach which could enable integration of in particular a CMOS VCO is use of a dual conversion receiver in which channel selection is performed by a second VCO running at a low frequency [1]. The first VCO where frequency is fixed can achieve low phase noise by using a wideband PLL [2] and a small varactor [3]. However, this architecture requires a wide tuning range for the second VCO. A 50% tuning range may be required to perform channel selection as well as to deal with process and temperature variations.

The desired wide tuning range can be achieved by using a ring oscillator, but it usually have poor phase noise [4]. On the other hand, use of an LC-VCO with a wide tuning range requires high VCO gain (MHz/V), especially at low supply voltages, which subsequently renders VCO more susceptible to the voltage noise induced phase noise [5].

In this paper, a 900 MHz CMOS VCO fabricated in a 0.18- μ m foundry process with an over 53% tuning range is presented. The VCO utilizes a switched resonator concept [6], which allows a reduction in the VCO gain. At 1.5 V power supply voltage, the VCO achieves -123 dBc/Hz phase noise at a 600 kHz offset frequency over the whole tuning range. Phase noise of -79 dBc/Hz at 10 kHz offset also can be extrapolated from the data at 100 kHz offset using 30 dB/dec frequency dependence. This phase noise is adequate for 802.11a wireless LAN application.

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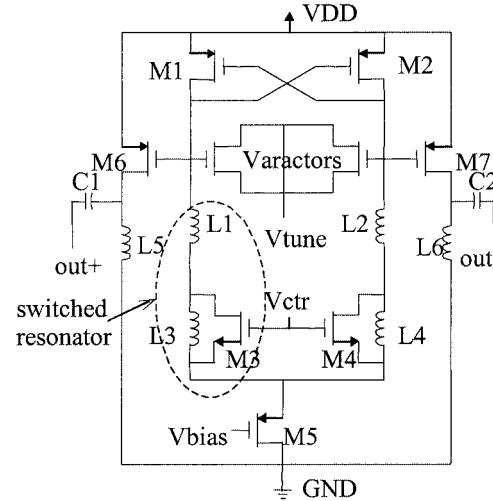


Fig. 1. VCO schematic including switchable $L-C$ resonators.

II. DESIGN OF VCO

A. Switching Inductor Concept

A high tuning range VCO has been attempted by varying inductance [7] with very poor phase noise outcome. As mentioned, in this work, the switched resonator concept illustrated in Fig. 1 is utilized to increase the tuning range and to achieve low phase noise over the tuning range at a reasonable power consumption. The inductance seen between ports 1 and 2 are changed by turning $M3$ on and off. When the transistor is off, the inductance is approximately the sum of $L1$ and $L2$. The actual combined inductance is somehow lower due to the effects of C_{GD} in series with C_{GS} , and C_{DB} of $M1$ [6]. These capacitances also affect the capacitance seen from $L1$ side (C_{p1}). When $M3$ is on, $L2$ is shunted out and the inductance is decreased. Furthermore, when $M3$ is on, C_{p1} is reduced because the transistor capacitances and the capacitances associated with $L1$ (partially) and $L2$ are shunted to ground by the low on-resistance of $M3$, thus, leading to simultaneous decreases of inductance and capacitance. This ability to simultaneously tune L and C provides greater flexibility to tradeoff phase noise and power consumption, as well as to achieve given phase noise performance over a larger frequency range [6] compared to using only switched capacitors [8].

B. VCO Circuit Design

The VCO schematic in Fig. 1 is similar to [6] and [9]. $M1$ and $M2$ are cross-coupled and provide negative resistances for

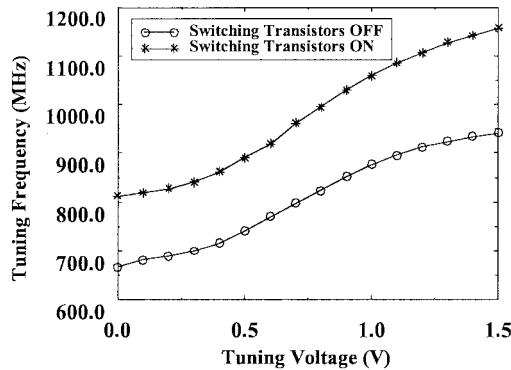


Fig. 2. VCO tuning characteristics: coarsely tuned by switching inductors and finely tuned by varactors.

the VCO core. The PMOS, $M5$ is used to set the current for the VCO. The sizes are $300/0.18 \mu\text{m}$ for $M1$, $M2$ and $2000/0.18 \mu\text{m}$ for $M5$. Having this large size for $M5$ reduces $1/f$ noise in the tail transistor and, thus, the close in phase noise of the VCO.

The LC tanks include MOS varactors, inductors, and variable resonator transistors $M3$ and $M4$. $L1$ and $L2$ are 2.5-nH inductors, and $L3$ and $L4$ are 1.2-nH inductors. The inductors have patterned ground shields [10], [11] and are formed by shunting metal 4, 5, and 6 layers. When control voltage ($Vctr$) is low, i.e., the switching transistors $M3$ and $M4$ are off, the total inductance of the tanks is around $2.5 + 1.2 = 3.7\text{ nH}$. When $Vctr$ is high, $M3$ and $M4$ shorts out $L3$, and $L4$, then the total inductance is approximately 2.5 nH . In this case, the on-resistances of $M3$ and $M4$ are series with $L1$ and $L2$, respectively, which increases resistance thus lowering inductor Q . In order to keep this detrimental effect small, $2000/0.18 \mu\text{m}$ NMOS transistors are used for $M3$ and $M4$. Simulations show that the on-resistance is 0.4Ω . The varactors are implemented using a MOS capacitors [12] and laid out using a differential architecture [13].

III. EXPERIMENTAL RESULTS

The VCO operates between 667 MHz to 1156 MHz , which is 53.6% tuning range. As shown in Fig. 2, the VCO is coarsely tuned with switched resonators and finely tuned using MOS varactors. When the switching transistors $M3$ and $M4$ are off, i.e., when $Vctr$ is low, by changing the MOS varactor tuning voltage ($Vtune$), the output frequency is varied from 667 to 942 MHz (Band 1). When the switching transistors are on or VGS of $M3$ and $M4$ is 1.5 V , the varactor tunes VCO from 813 to 1156 MHz (Band 2). There is a 130-MHz overlap between bands 1 and 2. This overlap ensures the continuity of tuning despite the process and temperature variations.

The VCO core draws about 14 mA , while the VCO buffer draws about 3 mA from a 1.5 V power supply. The output power is -1.67 dBm at the 1127 MHz center frequency. Fig. 3 shows the phase noise at a 600 kHz offset versus oscillation frequency. The phase noise is $-123\text{--}124\text{ dBc/Hz}$, which is good. More importantly, the phase noise is essentially flat over the entire operating frequency range.

Table I summarizes phase noise performances for bands 1 and 2. As mentioned previously, when switching transistors $M3$ and $M4$ are on, additional series resistances arising from the transistors could increase VCO phase noise. The conditions (b) and

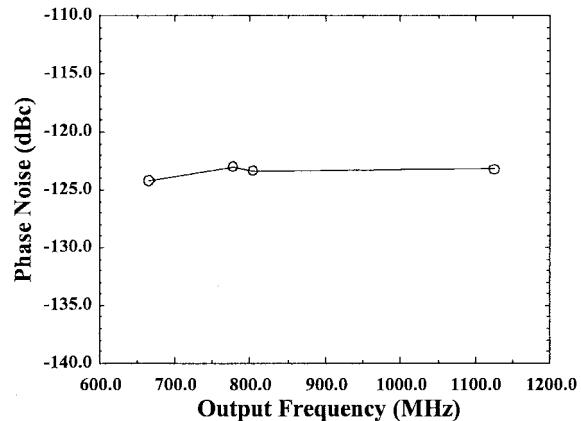


Fig. 3. VCO phase noise over output frequency range.

TABLE I
SUMMARY OF VCO CHARACTERISTICS

	(a)	(b)	(c)	(d)
$Vctr$ (V)	2.4	2.4	0	0
$Vtune$ (V)	1.5	0	0.8	0
Centre frequency (MHz)	1125	804	777	666
Phase Noise at 600 kHz offset (dBc/Hz)	-123.1	-123.3	-123	-124.2
Core Current (mA)	14.1	14.5	14.5	14.4

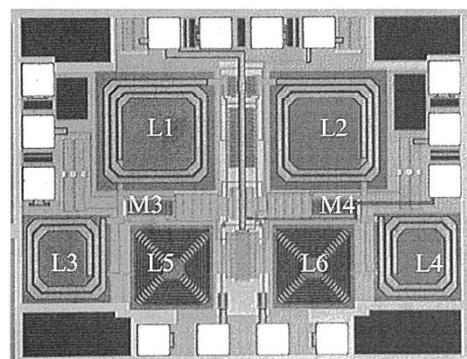


Fig. 4. VCO chip microphotograph.

(c) attempted to tune the VCO at the same frequency with the switching transistors on [case (b)] and off [case (c)]. Surprisingly, the resulting phase noise difference is less than 0.3 dB which is well within typical measurement tolerances. It appears that the on-resistances and other losses associated with the switch transistors can be made sufficiently low. This VCO has sufficient a tuning range and margins to be used for 802.11a applications with a 200-MHz band width (5.15 to 5.35 GHz). The phase noise measurements at 100 and 600 kHz offsets indicate that the VCO should be adequate for this application. Fig. 4 is a VCO chip microphotograph. It occupies $1100 \times 860 \mu\text{m}^2$.

IV. CONCLUSIONS

A 900-MHz monolithic VCO using switched resonators implemented in a $0.18\text{-}\mu\text{m}$ foundry CMOS process is presented. When operated under 1.5 V power supply, it achieves a 53.6% tuning range. Nearly constant phase noise of $-123\text{--}124$ dBc/Hz was observed over the entire tuning range between 667 MHz to 1156 MHz. At the 100 kHz offset, phase noise is around -109 dBc/Hz. These phase noise performance should be sufficient for numerous RF applications.

REFERENCES

- [1] J. Rudell, J. J. Ou, T. Cho, G. Chien, F. Brianti, J. Weldon, and P. Gray, "A 1.9 GHz wide-band IF double conversion CMOS receiver for cordless telephone applications," *IEEE J. Solid-State Circuits*, vol. 32, pp. 2071–2087, Dec. 1997.
- [2] L. Lin, L. Tee, and P. Gray, "A 1.4 GHz differential low-noise CMOS frequency synthesizer using a wideband PLL architecture," in *ISSCC Dig. Tech. Papers*, 2000, pp. 204–205.
- [3] E. Hegazi, H. Sjoland, and A. A. Abidi, "A filtering technique to lower oscillator phase noise," in *ISSCC Dig. Tech. Papers*, 2001, pp. 364–365.
- [4] C. Park and B. Kim, "A low-noise 900MHz VCO in $0.6\mu\text{m}$ CMOS," in *VLSI Circuits Symp. Dig. Tech. Papers*, 1998, pp. 28–29.
- [5] B. D. Muer, N. Itoh, M. Borremans, and M. Stayaert, "A 1.8 GHz highly-tunable low-phase-noise CMOS VCO," in *Proc. CICC*, 2000, pp. 585–588.
- [6] S. Yim and K. K. O, "Demonstration of a switched resonator concept in a dual-band monolithic CMOS LC-tuned VCO," in *Proc. CICC*, 2001, pp. 205–208.
- [7] F. Herzel, H. Erzgraber, and N. Ilkov, "A new approach to fully integrated CMOS LC-oscillators with a very large tuning range," in *Proc. CICC*, 2000, pp. 573–576.
- [8] J. Mourant, J. Imbornone, and T. Tewksbury, "A low phase noise monolithic VCO in SiGe BiCMOS," in *RFIC Symp. Dig. Papers*, 2000, pp. 65–68.
- [9] C.-M. Hung and K. K. O, "A packaged 1.1 GHz CMOS VCO with phase noise of -126 dBc/Hz at a 600 kHz offset," *IEEE J. Solid-State Circuits*, vol. 35, pp. 100–103, Jan. 2000.
- [10] C. P. Yue and S. S. Wang, "On-chip spiral inductors with patterned ground shields for Si-based RF ICs," *IEEE J. Solid-State Circuits*, vol. 33, pp. 734–752, May 1998.
- [11] S.-M. Yim, T. Chen, and K. K. O, "The effects of a ground shield on spiral inductors fabricated in a silicon bipolar technology," in *Proc. Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, Sept. 2000, pp. 157–160.
- [12] C.-M. Hung, Y.-C. Ho, I.-C. Wu, and K. K. O, "High- Q capacitors implemented in a CMOS process for low-power wireless applications," *IEEE Trans. Microwave Theory Tech.*, vol. 46, pp. 505–511, May 1998.
- [13] A. Porret, T. Melly, C. Enz, and E. A. Vittoz, "Design of high- Q varactors for low-power wireless applications using a standard CMOS process," *IEEE J. Solid-State Circuits*, vol. 35, pp. 337–345, Mar. 2000.